US-PAT-NO: 5973335

DOCUMENT-IDENTIFIER: US 5973335 A

TITLE: Semiconductor memory devices with amorphous silicon alloy

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Brief Summary Text - BSTX (15):
The programming process preferably comprises a current stressing operation in which an electric current is passed through the structure, using the two conductive contact layers as terminals, at a current density sufficient to create a defect band. In this case, the region of the structure, or more particularly the region of the alloy layer, upon which the programming process is performed is that through which the electrical current flows. The defects in the defect band comprise silicon dangling bonds in the region of the valence band in the alloy. By varying the magnitude of the electrical current, and/or the time for which it is applied, the activation energy level of the device in subsequent use can be predetermined and selected from a range of possible values, thereby programming the device. The activation energy level decreases progressively in accordance with, for example, an increase in the applied current stressing time, assuming constant current density. The creation of a defect band distinguishes the device from the known kind of memory devices in which localised filaments are produced in the amorphous silicon layer through the forming process.

Detailed Description Text - DETX (12):
One possible explanation for the effects of such current stressing in the TFD device will now be given. The defect band induced by current stressing enables current to flow from anode to cathode in parallel with the current passing over the potential barrier. The shift in the I-V characteristic at higher applied voltages observed after stressing is almost symmetric which suggest that the electric field in both arms has been reduced by approximately

| | U | I | Document ID | Issue Date | Pages | Tit |
|---|---|---|---|---|---|---|
| 40 | ☐ | ☐ | US 5973335 A | 19991026 | 18 | Semiconductor memory devices wi |
| 41 | ☐ | ☐ | US 5970316 A | 19991019 | 12 | Method of making active pixel s leakage current |
| 42 | ☐ | ☐ | US 5958340 A | 19990928 | 9 | Solid-state chemical sensor |
| 43 | ☐ | ☐ | US 5943552 A | 19990824 | 30 | Schottky metal detection method |
| 44 | ☐ | ☐ | US 5917195 A | 19990629 | 31 | Phonon resonator and method for |

# United States Patent [19]

Shannon

[11] Patent Number: 5,973,335

[45] Date of Patent: *Oct. 26, 1999

[54] SEMICONDUCTOR MEMORY DEVICES WITH AMORPHOUS SILICON ALLOY


[75] Inventor: John M. Shannon, Whyteleafe, United Kingdom

[73] Assignee: U.S. Philips Corporation, New York, N.Y.


[*] Notice: This patent issued on a continued prosecution application filed under 37 CFR 1.53(d), and is subject to the twenty year patent term provisions of 35 U.S.C. 154(a)(2).


[21] Appl. No.: 08/574,809

[22] Filed: Dec. 19, 1995

[30] Foreign Application Priority Data

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Aug. 3, 1995 [GB] United Kingdom ..... 9515961

[51] Int. Cl.* ..... H01L 39/04; H01L 31/036

[52] U.S. Cl. ..... 257/49; 257/52; 257/53; 257/54; 257/63; 257/70; 257/72; 257/196; 365/129

[58] Field of Search ..... 257/49, 52–54, 257/63, 70, 72, 196, 530; 365/129



[56] References Cited

U.S. PATENT DOCUMENTS

| | | | |
|---|---|---|---|
| 3,611,063 | 10/1971 | Neale | 257/530 |
| 4,217,374 | 8/1980 | Ovshinsky et al. | 427/39 |
| 4,226,898 | 10/1980 | Ovshinsky et al. | 427/39 |
| 4,488,262 | 12/1984 | Basire et al. | 257/530 |
| 4,499,557 | 2/1985 | Holmberg et al. | 257/530 |
| 4,599,705 | 7/1986 | Holmberg et al. | 257/530 |
| 4,858,515 | 8/1989 | Johnson et al. | 257/63 |
| 5,210,766 | 5/1993 | Winer et al. | 257/52 |
| 5,233,206 | 8/1993 | Lee et al. | 257/530 |
| 5,293,335 | 3/1994 | Perrias et al. | 257/2 |
| 5,367,392 | 11/1994 | Janal | 257/72 |
| 5,477,482 | 12/1995 | Prinz | 365/129 |

FOREIGN PATENT DOCUMENTS

| | | | |
|---|---|---|---|
| 0588402 | 3/1994 | European Pat. Off. | G11C 17/14 |
| 9000817 | 1/1990 | WIPO . | |
| 9013921 | 11/1990 | WIPO . | |

OTHER PUBLICATIONS

"Metal–Semiconductor Transition in Electroformed Chromium:Amorphous Silicon/Vanadium Thin–Film Structures", by J. Hajto et al, Philosophical Magazine B., 1994, vol. 69, No. 2, 237–251.



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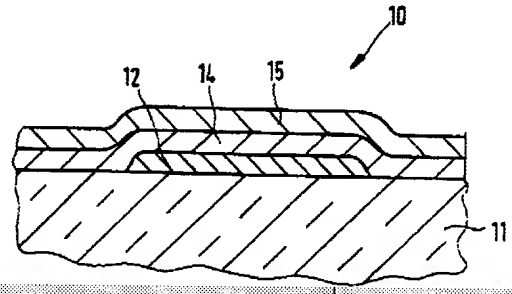
[57] ABSTRACT


A semiconductor memory device includes first and second conductive contact layers (12, 15) and an hydrogenated, silicon-rich, amorphous silicon alloy layer (14), particularly an amorphous silicon nitride or amorphous silicon carbide alloy, extending between the contact layers. A defect band is induced in the amorphous silicon layer which lowers the activation energy level for the transport of carriers through the structure by an amount that is selectable and determined by the defect band. The defect band is created by a programming process, for example, using current stressing or particle bombardment. A memory matrix array device is provided by forming a row and column array of such memory devices from common deposited layers on a common substrate with crossing sets of row and column conductors separated by a layer of the alloy material defining a memory device at each of their cross-over regions. A plurality of overlying arrays of memory devices may be stacked on the support to provide a 3-D memory structure in a simple manner.


15 Claims, 5 Drawing Sheets

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